Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.303”**

**.181”**

**G**

**SOURCE**

**SOURCE**

**G = GATE**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: Gate = .021” X .021”**

**Backside Potential: Drain**

**HEX – 4.6 150-200V**

**N-Channel GEN 5.3**

**APPROVED BY: DK DIE SIZE .181” X .303” DATE: 7/11/22**

**MFG: IR THICKNESS .014” P/N: IRFC42N20DB**

**DG 10.1.2**

#### Rev B, 7/19/02